Notice of Allowability	Application No.	Applicant(s)	
	10/707,845	BONGES ET AL.	
	Examiner	Art Unit	
	Helen Rossoshek	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Amendment filed 05/01/2006*.

2. ☒ The allowed claim(s) is/are *1-20*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *07/05/2006* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

JACK CHIANG
SUPERVISORY PATENT EXAMINER

DETAILED ACTION

1. This office action is in response to the Application 10/707,845 filed 01/16/2004 and amendment filed 05/01/2006.

2. Claims 1-20 remain pending in the Application.

3. Applicant's arguments have been fully considered and are persuasive.

EXAMINER'S AMENDMENT

4. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

5. Authorization for this examiner's amendment was given in a telephone interview with Spencer Warnick (Registration No. 40,398) on 07/05/2006.

6. The application has been amended as follows:

To claims

Claim 16 line 2 after "therein" delete "for" insert –when executed performs--

Allowable Subject Matter

7. Claims 1-20 are allowed. The following is an examiner's statement of reasons for allowance: The prior art of record does not teach a method, system and computer program product for merging an original integrated circuit shape and at least one overlapping clone of the original integrated circuit shape of an integrated circuit design, including determination whether each corner point of each overlapping clone of the original integrated circuit shape is within a threshold distance of a corresponding original

corner point of the original integrated circuit shape; and when each clone corner of each overlapping clone is within the threshold distance, generate a union of each overlapping clone and the original circuit shape, such that the union does not contain a notch.

8. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Scheffer (US Patent Application Publication 20050246675) discloses a method for modifying an upper layout for an upper layer of an IC using information including modifications made to geometries in the IC layout (and **replicated** on a photomask) to adjust for the errors in the resulting geometries fabricated on the wafer, wherein modifications are made to **original geometries** to produce only satisfactory **resulting/duplicated geometries** that are within an allowable threshold of variance from the original geometries, but lacks a method, system and computer program product for merging an original integrated circuit shape and at least one overlapping clone of the original integrated circuit shape of an integrated circuit design, including determination whether each corner point of each overlapping clone of the original integrated circuit shape is within a threshold distance of a corresponding original corner point of the original integrated circuit shape; and when each clone corner of each overlapping clone is within the threshold distance, generate a union of each overlapping

clone and the original circuit shape, such that the union does not contain a notch. Cohn et al. (US Patent Application Publication 20050262463) discloses a method of designing electrical structure in an integrated circuit design including actions of **cloning** (duplicating a circuit and distributing its fanout between the original circuit and the copy), factoring, pin swapping, etc, but lacks a method, system and computer program product for merging an original integrated circuit shape and at least one overlapping clone of the original integrated circuit shape of an integrated circuit design, including determination whether each corner point of each overlapping clone of the original integrated circuit shape is within a threshold distance of a corresponding original corner point of the original integrated circuit shape; and when each clone corner of each overlapping clone is within the threshold distance, generate a union of each overlapping clone and the original circuit shape, such that the union does not contain a notch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Helen Rossoshek whose telephone number is 571-272-1905. The examiner can normally be reached on 7:30-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Examiner
Helen Rossoshek
AU 2825

JACK CHIANG
SUPERVISORY PATENT EXAMINER